G.728

DSP-BASED SPEECH COMPRESSION CODER

nalog Devices' G.728 full-duplex speech compression coder, running on a high-performance 33 MIPS Digital Signal Processor (DSP), compresses the speech or any other audio signal component of multimedia software or other audio. This speech coder chipset includes software code which conforms to the ITU H.320 standards family. In addition, acoustic echo cancellation is a standard feature.

The speech coder chipset features a 16 kbps bit rate using low-delay code-excited linear prediction (LD-CELP). The coder uses an analysis-by-synthesis approach to codebook search. LD-CELP uses backward adaptation of predictors and gain to reduce the algorithmic delay to 0.625 msec.

The coder includes independent gain control with 256 steps, independent audio mode muting, multi-stage loopback modes for testing and a seamless acoustic echo cancellation interface.

The G.728 chipset includes an ADSST-G728-xxxx, 33-MIPS Digital Signal Processor. The G.728 software code requires 20 MIPS, 8 KWords PM RAM and 12 KWords DM RAM of the DSP. A demonstration featuring the G.728 compression algorithm with or without acoustic echo cancellation is available to run on an Analog Devices EZ-LITE development board.

ANALOG DEVICES WORLDWIDE HEADQUARTERS

One Technology Way P.O. Box 9106 Norwood, MA 02062-9106 USA

tel: 617 461 3060 fax: 617 461 4360

email: systems.solutions@analog.com

HIGHLIGHTS

- 16 kbps Bit Rate
- Discontinuous Transmission And Noise Fill During Non-Speech Intervals
- Optimizer Represented In Speech
- Encodes Speech Using Low-Delay Code-Excited Linear Prediction (LD-CELP)
- Frame Size: 30 msec
- Delay Time: 7.5 msec
- Minimum Buffer Size: 2.5 msec

The frame size is 30 msec and there is an additional look-ahead of 7.5 msec, resulting in a total algorithmic delay of 37.5 msec.

The speech coder may be used in Digital Circuit Multiplication Equipment (DCME) systems. In such systems, the digital speech interpolation (DSI) sections removes silent intervals from speech. The adaptive-dfferential pulse-code modulation (ADPCM) component compresses 64 kbit/sec speech to 32 kbit/sec, effectively representing each sample using 4 bits, compared to companded PCM which uses 8 bits per sample.

The G.728 speech coder has an effective minimal buffer size of 2.5 msec, which can be increased to accommodate any size without affecting the core algorithm.

This chipset is available with and without Acoustic Echo Cancellation and can be ordered under part numbers ADSST-G728-xxxx. License agreements must be signed before delivery of the chipset.